IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~ or double brackets [[ ]].

Please REPLACE paragraph [0052] on page 11 with the following amended paragraph:

[0052] The driving TFT 200 is connected to the power supply line 140 and the storage capacitor 180, and serves to drive the organic EL element 300. The driving TFT 200 includes a semiconductor layer 210, a gate electrode 220, a source electrode 250, and a drain electrode 255. The gate electrode 220 of the driving TFT 200 extends from the first capacitor electrode 182, and the source electrode 250 of the driving TFT 200 extends from the power supply line 140. The source and drain electrodes 250 and 255 directly contact the semiconductor layer 210, without contact holes. The drain electrode 255 of the driving TFT 200 ~~contact~~ contacts an anode 310 of the organic EL element 300 through an opening portion 267 (shown in FIGS. 5C-5E). As such, the driving TFT 200 is electrically connected to the organic EL element 300.

Please REPLACE paragraphs [0064], [0065], and [0066] on page 13 with the following amended paragraphs:

[0064] Since the high-density impurity is ion-implanted into the semiconductor ~~layer~~ layers 172 and ~~220~~ 210 through the silicide layers 240, the semiconductor layers 172 and 210 [[is]] are protected by the silicide layers 240, thereby minimizing damage to the semiconductor ~~layer~~ layers 172 and 210 due to the ion-implantation.

[0065] Finally in FIG. 5A, a metal layer for source and drain electrodes is deposited over the whole surface of the substrate 110 and then patterned using a third mask to form the source and drain electrodes 250 and 255. The source and drain electrodes 250 and 255 directly contact the high-density source and drain regions 216-1 and 216-2 through the silicide layers 240, respectively, and without the contact holes 19-1 and 19-2 shown in FIG. 1.

[0066] At the same time, the source and drain electrodes 176 and 178 of the switching TFT 170 (see FIG. 6) are formed to directly contact the high-density source and drain regions 175-1 and 175-2 through the silicide layers 240, respectively. Even though not shown, the data line 130 and the power supply line 140 are also formed at the same time (referring to FIG. [[6]] 4).

Please REPLACE paragraph [0075] on pages 14-15 with the following amended paragraph:

[0075] As described above, the active matrix display device according to the embodiments of the present invention have the following advantages. Since the source and drain electrodes directly contact the source and drain regions without contact holes, the number of [[a]] mask ~~process~~ processes is reduced, thereby simplifying a manufacturing process. Furthermore, since only ~~five-mask~~ five mask processes are required to manufacture the active matrix display device, the overall manufacturing process is simplified, leading to a higher manufacturing yield and a lower production cost. Also, since the capping layer is formed on the gate electrode of the TFT while an ion-implanting process is performed to form the low-density source and drain regions, damage to the gate electrode is prevented. In addition, due to the silicide layers respectively formed between the source and drain regions and the source and drain electrodes, a contact resistance is reduced, leading to a high reliability. In addition, since an LDD region or an off-set region is formed in a ~~self-align~~ self-aligning manner through the spacers formed on both sidewall portions of the gate electrode and the capping layer, the manufacturing process is again simplified, and the electric characteristics such as an on/off current ratio [[is]] are improved.